Amendments to the Claims:

This listing of the claims shall replace all previous versions and listings of the claims.

Listing of Claims

1. (Currently Amended) A radio frequency (RF) multi-antenna access point system implemented in a single chip integrated circuit chip (IC) comprising:

a baseband processor circuit located in a first portion of the single chip IC ~~for handling~~ , the baseband processor circuit to handle data transmissions during a first operating mode in a channel between a first access point and a second access point; and

a multi-antenna signal processing circuit located in a second portion of the single chip IC ~~for handling~~ , the multi-antenna signal processing circuit to handle data transmissions during a second operating mode in said channel, said multi-antenna signal processing circuit being further adapted to: (a) receive M independent RF modulated input signals from said second access point; and (b) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point;

wherein said first operating mode and said second operating mode are to be automatically selected by the RF multi-antenna access point system based on a transmission condition in said channel.

2. (Original) The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit includes an analog to digital converter, and a digital to analog converter for interfacing to an antenna.

3. (Original) The RF multi-antenna access point system of claim 2, wherein said multi-antenna signal processing circuit includes a Fast Fourier Transform (FFT) Circuit.

4. (Original) The RF multi-antenna access point system of claim 3, wherein said multi-antenna signal processing circuit includes a preamble acquisition circuit for performing a preamble acquisition to align an FFT data frame with an 802.11x based data stream.

5. (Currently Amended) The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit is to process ~~processes~~ at least 4 separate input signals representing a data stream multiplexed over 4 separate bit streams.

6. (Currently Amended) The RF multi-antenna access point system of claim 1, wherein said channel mixing matrix is to compute ~~performs an operation that computes~~ a recovered data signal x as follows:

$$x=b1*y1+b2*y2+x0,$$

where b1 and b2 are equalization coefficients to be computed by said multi-antenna signal processing circuit, y1 and y2 are received data from separate baseband channels, and x0 is a recovered signal from an adjacent integrated circuit ~~channel~~.

7. (Currently Amended) The RF multi-antenna access point system of claim 1, wherein space division multiple access is to be realized by separating different RF signals from different directions simultaneously in the single chip IC.

8. (Currently Amended) The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit is to extend ~~extends~~ a data transmission range that can be achieved by said baseband processor circuit between said first access point and said second access point.

9. (Currently Amended) The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit is to increase ~~increases~~ a data transmission rate that can be achieved by said baseband processor circuit between said first access point and said second access point.

10. (Currently Amended) The RF multi-antenna access point system of claim 1, wherein said multi-antenna signal processing circuit is to transmit ~~transmits~~ M separate data signals to said second access point.

11. (Currently Amended) The RF multi-antenna access point system of claim 10, wherein a localized encryption is to be achieved for said second access point by independently controlling said M separate transmission signals.

12. (Original) The RF multi-antenna access point system of claim 1, wherein said first access point can be configured during a data transmission to transmit with an energy level which is substantially the same as a noise level to locations other than a localized region where said second access point is located.

13. (Currently Amended) An 802.11x compatible radio frequency (RF) multi-antenna access point enhancement circuit implemented in a single chip integrated circuit (IC) comprising:

a multi-antenna signal processing circuit situated in a first portion of the single chip IC and configured as a first access point adapted to: (a) operate simultaneously with a first baseband processor situated in a second portion of the single chip IC, so that said first baseband processor handles data transmissions in a first mode between said first access point, in accordance with an 802.11x protocol, and a second access point under a first channel transmission condition, and said multi-antenna signal processor handles data transmissions in a second mode between said first access point and said second access point in accordance with an 802.11x protocol under a second channel transmission condition; (b) receive M independent RF modulated input signals from said second access point when the second channel transmission mode exists between the first access point and said second access point; (c) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point; (d) transmit an RF modulated signal to said second access point using a point coordination function (PCF) mode associated with said 802.11x protocol so as to maintain timing compatibility; wherein said multi-antenna signal processing circuit operates with a first baseband processor to receive and transmit RF signals in a channel between said first access point and said second access point.

14. (Currently Amended) The circuit of claim 13, wherein said multi-antenna signal

processing circuit is to process ~~processes~~ data using a high rate direct sequence spread spectrum (HR/DSSS) physical layer frame structure that has a preamble and header compatible with said 802.11x protocol.

15. (Original) The circuit of claim 13, wherein said header includes additional data to identify a high rate mode.

16. (Original) The circuit of claim 13, wherein said header includes additional data to identify a modulation format.

17. (Currently Amended) The circuit of claim 13, wherein said first baseband processor [[sends]] is to send multicast transmissions to a first set of targets within a first range of said first access point, and said multi-antenna signal processing circuit [[sends]] is to send multicast transmissions to a second set of targets within a second range of said first access point.

18. (Currently Amended) The circuit of claim 13, wherein first baseband processor ~~communicates~~ is to communicate with a first set of targets during a first access period, and said multi-antenna signal processing circuit is to communicate ~~communicates~~ with a second set of targets during a second access period.

19. (Currently Amended) The circuit of claim 18, wherein said first access period and said second access period are to be alternated at a predetermined ratio.

20. (Currently Amended) The circuit of claim 13, wherein said multi-antenna signal processing circuit [[uses]] is to use a wave beam transmission to communicate selectively to a target in a specific location[,] and not to other targets.

21. (Currently Amended) The circuit of claim 13, wherein said multi-antenna signal processing circuit is incorporated as part of a closed circuit television monitoring system, and said M independent signals are to be transmitted by N individual cameras.

22. (Currently Amended) The circuit of claim 13, wherein a receive sensitivity of said first access point [[can]] is to be improved by selectively adding additional multi-antenna signal processing circuit modules for a data transmission[[,]] and/or increasing M.

23. (Original) A single chip integrated circuit (IC) radio frequency (RF) multi-antenna access point circuit comprising:

a baseband processor circuit in the single chip IC to handle ~~for handling~~ data transmissions during a first operating mode in a channel between a first access point and a second access point;

a multi-antenna signal processing circuit in the single chip IC to handle ~~for handling~~ data transmissions during a second operating mode in said channel, said multi-antenna signal processing circuit being further adapted to: (a) receive M independent RF modulated input signals from said second access point; (b) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data

signals transmitted by said second access point[[;]], wherein said first operating mode and said second operating mode are to be automatically selected by the RF multi-antenna access point system based on a transmission condition in said channel;

a modulator/demodulator circuit in the single chip IC to be coupled to an antenna assembly and said multi-antenna signal processing circuit and baseband processor circuit to extract ~~for extracting~~ I/Q data samples from an RF modulated received signal;

a media access controller in the single chip IC coupled to said multi-antenna signal processing circuit and baseband processor circuit to interface ~~for interfacing~~ to a host computing system.

24. (Currently Amended) A system in an integrated circuit chip (IC) comprising:

a baseband processor circuit located in a first portion of the IC and capable of handling data transmissions during a first operating mode; and

a multi-antenna signal processing circuit located in a second portion of [[a]] the IC and capable of handling data transmissions during a second operating mode, wherein the multi-antenna signal processing circuit is not utilized during the first operating mode.

25. (Cancelled)

26. (Currently Amended) A system in an IC according to claim [[25]] 24, wherein the multi-antenna signal processing circuit is capable of processing [[the]] M independent modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by an ~~the second~~ access point.

27. (Currently Amended) A system in an IC according to claim 24, wherein the first operating mode [[or]] and the second operating mode are to be selected by the multi-antenna signal processing circuit ~~access point system~~ based at least on a transmission condition in the channel.

28. (Currently Amended) A system in an IC according to claim 24, wherein the multi-antenna signal processing circuit comprises an analog to digital converter or a digital to analog converter, or ~~cobinations~~ combinations thereof, being capable of interfacing to an antenna.

29. (Previously Presented) A system in an IC according to claim 24, wherein the multi-antenna signal processing circuit comprises a Fast Fourier Transform (FFT) Circuit.

30. (Previously Presented) A system in an IC according to claim 29, wherein the multi-antenna signal processing circuit comprises a preamble acquisition circuit capable of performing a preamble acquisition to align an FFT data frame with an IEEE 802.11 type based data stream.

31. (Currently Amended) A system in an IC according to claim 24, wherein the multi-antenna signal processing circuit is capable of ~~processesing~~ processing at least 4 separate input signals representing a data stream multiplexed over 4 separate bit streams.

32. (Currently Amended) A system in a single chip IC according to claim 24, wherein the multi-antenna signal processing circuit ~~channel mixing matrix~~ is capable of computing ~~performing an operation that computes~~ a recovered data signal x as follows:

$x=b_1*y_1+b_2*y_2+x_{0,}$

where b_1 and b_2 are equalization coefficients to be computed by the multi-antenna signal processing circuit, y_1 and y_2 are received data from separate baseband channels, and x_0 is a recovered signal from another IC ~~an adjacent channel~~.

33. (Currently Amended) A system in an IC according to claim 24, wherein space division multiple access is to be realized by separating signals from different directions simultaneously or nearly simultaneously in the IC.

34. (Currently Amended) A system in an IC according to claim 24, wherein the multi-antenna signal processing circuit is capable of extending a data transmission range that can be achieved by the baseband processor circuit between a first access point and a second access point.

35. (Currently Amended) A system in an IC according to claim 24, wherein the multi-antenna signal processing circuit is to increase ~~increases~~ a data transmission rate that can be achieved by the baseband processor circuit between a first access point and a second access point.

36. (Currently Amended) A system in an IC according to claim [[25]] 24, wherein the multi-antenna signal processing circuit is capable of transmitting M separate data signals to an ~~the second~~ access point.

37. (Currently Amended) A system in an IC according to claim 36, wherein a localized encryption is capable of being achieved for the ~~second~~ access point by independently controlling the M separate transmission signals.

38. (Currently Amended) A system in an IC according to claim [[25]] 24, wherein ~~the first~~ an access point incorporating said IC is capable of being configured during a data transmission to transmit with an energy level which is substantially the same as a noise level to locations other than a localized region to which the data transmission is directed ~~where the second access point is located~~.

39. (Previously Presented) A system in an IC according to claim 24, wherein the multi-antenna signal processing circuit is compatible with an IEEE 802.11 type standard.

40. (Currently Amended) A system in an IC according to claim 24, wherein the multi-antenna signal processing circuit is capable of operating simultaneously with the first baseband processor and wherein the first baseband processor is capable of handling data transmissions in a first mode between the first access point ~~in accordance~~ and a second access point under a first channel transmission condition.

41. (Currently Amended) A system in an IC according to claim 40, wherein the multi-antenna signal ~~processor~~ processing circuit is capable of handling data transmissions in the second mode between a first access point and a second access point in accordance with an IEEE 802.11 type protocol under the second channel transmission condition.

42. (Currently Amended) A system in an IC according to claim 41, wherein the multi-antenna signal ~~processor~~ processing circuit is capable of receiving M independent modulated input signals from the second access point when the second channel transmission mode exists between the first access point and the second access point.

43. (Currently Amended) A system in an IC according to claim 41, wherein the multi-antenna signal ~~processor~~ processing circuit is capable of transmitting modulated signals to the second access point using a point coordination function (PCF) mode associated with the 802.11 type protocol.

44. (Currently Amended) A system in an IC according to claim 24, wherein the multi-antenna signal processing circuit is capable of operating with the first baseband processor to receive and transmit signals in a channel between [[the]] a first access point and [[the]] a second access point.

45. (Currently Amended) An integrated circuit (IC) comprising:

a baseband processor circuit capable of handling data transmissions during a first operating mode in a channel between a first access point and a second access point; and

a multi-antenna signal processing circuit capable of handling data transmission during a second operating mode in the channel, wherein the multi-antenna signal processing circuit is not utilized during the first operating mode.

46. (Currently Amended) An IC according to claim 45, further comprising:

a modulator/demodulator circuit to be coupled to an antenna assembly and the multi-antenna signal processing circuit and baseband processor circuit; and

a media access controller coupled to the multi-antenna signal processing circuit and baseband processor circuit and capable of interfacing to a host computing system.